

RELATED APPLICATION DATA

The present application claims priority under 35 U.S.C. § 119 to U.S. Provisional Application Serial No. 60/227944 (Attorney Docket No. FUNP001), naming James et al. as inventors, and filed August 25, 2000, the entirety of which is
5 incorporated herein by reference in its entirety for all purposes.

BACKGROUND OF THE INVENTION

The present invention is related generally to sequencing devices, and more particularly to the sequencing technique with automated active port detection and
10 sequencing.

Conventionally, sequencing circuits typically include a relatively small number of ports (e.g. 1-5 ports) for sequencing attached wires according to a predefined sequence. If more wires are needed to be sequenced, then two or more conventional sequencing units may be serially combined to produce a system which is able sequence
15 the desired number of wires. For this reason, conventional sequencers having a relatively large number of sequencing ports (e.g. more than 5) are uncommon, since it is cheaper to combine a few smaller sequencing units than to manufacture a large sequencing unit.

One problem with conventional sequencing units is that they are not able to
20 perform automatic wire detection. Without wire-detection, the device controlling the wires would produce "blanks" in the patterns, or points in the sequence where no wires are connected, when the sequencer attempts to turn on those wires. Another problem with conventional sequencing devices relates to zero-crossing issues, as described in greater detail in the Detailed Description Section of this application.

25 Accordingly, it will be appreciated that there exists a present need to improve upon conventional sequencing device designs in order to provide improved features and advantages.

SUMMARY OF THE INVENTION

According to various embodiment the present invention, methods, systems, and computer program products are disclosed for detecting active ports of an electronic device. The electronic device comprises a plurality of ports, including a first port. A
5 determination is automatically performed as to whether an external component is connected to the first port. The first port is identified as an active port in response to a determination that an external component is connected to the first port. If there no external component is connected to the first port, then the first port is identified as an inactive port. The inactive and active ports may then be distinguished and treated
10 differently during subsequent control and/or management of the plurality of ports. According to one implementation the first port may be identified as an active port in response to detection of a capacitive load connected to the first port. In a different implementation, the first port may be identified as an active port in response to detection of a resistive load connected to the first port. In an alternate implementation,
15 the first port as may be identified an active port in response to a determination that an inductive load is connected to the first port. In yet another implementation, the first port as may be identified an active port in response to a determination that a current is flowing through the first port.

Alternate embodiments of the present invention are directed to various methods,
20 systems, and computer program products for sequencing selected ports of an electronic device which includes a first port and a second port. Active ports of the electronic device are automatically identified. According to a specific embodiment, an active port may be characterized as a port which has an external load physically connected to it. Sequencing of only desired, active ports of the electronic device may then be
25 implemented.

Additional objects, features and advantages of the various aspects of the present invention will become apparent from the following description of its preferred embodiments, which description should be taken in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 shows a block diagram of a sequencing device 100 in accordance with a specific embodiment of the present invention.

Figures 2A and 2B shows a block diagrams of active port detection (APD) devices which have been implemented in accordance with specific embodiments of the present invention.

Figure 3 shows a schematic diagram illustrating a specific embodiment of the active port detection device 300 of the present invention.

Figure 4 shows a flow diagram of a Sequencing Initialization Procedure 400 in accordance with a specific embodiment of the present invention.

Figure 5 shows an example of an Active Port Table 500 in accordance with a specific embodiment of the present invention.

Figure 6 shows an example of an alternate implementation of the wire-detect circuit of Figure 2A.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows a block diagram of a sequencing device 100 in accordance with a specific embodiment of the present invention. As shown in the embodiment of Figure 1, the sequencing device 100 includes a plurality of ports 102, a sequencer 110, and an active port detection circuit 130. In a specific implementation, the active port detection circuit 130 may include a processing device 132 (e.g. a CPU, EEPROM, AISIC, etc.) and memory 134. As explained in greater detail below, the sequencing device 100 may be configured or designed to automatically detect the presence of one or more wires connected to one or more of the of the ports 102. Once the sequencing device has determined the specific ports which are active (e.g. ports which have wires connected to them), the sequencing device may then sequence each of the active ports, in a particular order without attempting to include inactive ports in the sequence. According to one implementation, the active port detection circuit 130 may be responsible for sequencing each of the active ports. In an alternate embodiment, the sequencer 110 may sequence the active ports using information provided by the active port detection circuit 130.

According to specific embodiments, the technique of the present invention provides a number of advantages and/or features which are not provided by

conventional sequencing devices. For example, the sequencing technique of the present invention may be used to provide automatic wire detection of wires attached to a sequencing unit. Because of this feature, a generic sequencing unit may be manufactured to have a relatively large number of ports (e.g. 5-10 or more ports), and the automatic wire detection feature may then be used to automatically detect and sequence only active ports (e.g. only those ports on the unit where a wire or circuit is physically connected).

According to a specific embodiment, and active port detection (APD) device of the present invention may be configured or designed to detect the presence of devices or elements which are physically connected to ports of the APD device. According to a specific implementation, the detection of the presence of an element, component, or device connected to a given port may be based upon detection of a capacitive load connected to the port. Alternatively, the detection of the presence of an element, component, or device connected to a given port may be based upon detection of a resistive load connected to the port. In another implementation, the detection of the presence of an element, component, or device connected to a given port may be based upon detection of current flowing through the port.

The APD device may be configured to detect the presence or absence of devices/elements connected to its ports upon power up (or reset). Thereafter, once the active ports have been identified, the APD device may be configured to control only the identified active ports. Empty or no-active ports may be selectively omitted from being controlled by the APD device. In a specific embodiment, the APD device corresponds to a sequencing device which may be configured or designed to sequence only active ports on the sequencing device. However, the technique of the present invention may be applied to applications other than sequencing operations. For example, a device which is configured to implement the active port detection technique of the present invention may be provided to allow a user to connect desired wires and/or circuits to one or more ports on the device, and the device may then automatically determine the active ports on the device, and use this information when performing future operations.

According to a specific embodiment, the APD device may be configured or designed to automatically detect the presence of elements which are physically connected to ports of the APD device, even when such elements do not form a closed

10-port APD device using any combination of six of the 10 ports. In this example, using the technique of a present invention, the physical sequencing of ports: P0, P3, P5, P6, P8, P9, for example, may be assigned a logical sequence of: Device 0, - Device 5.)

Additionally, if ports two and three were physically damaged, the user could connect devices to any of the eight remaining ports to produce a “logically” consecutive sequence of the active ports. Thus, unlike conventional techniques, physically damaged ports do not produce “blanks” in sequences. Moreover, the user can use another connector if a connector (port) aboard the APD device is physically damaged (i.e., pins are broken, electrical continuity to port is broken).

Figure 2A shows a block diagram of an APD device 200 which has been implemented in accordance with a specific embodiment of the present invention. It will be appreciated that the APD device of Figure 2A may be modified by one having ordinary skill in the art to include additional or fewer components than those illustrated in Figure 2A.

Referring now to the APD device 200 of Figure 2A, a power source (201) supplies power to a power converter (202) which converts the power from the power source to a voltage, current, and frequency sufficient to supply a load connected to a port (e.g. port 208a) of the circuit with power appropriate to cause this load to function (e.g., power appropriate to cause an L.E.D. to illuminate, power appropriate to cause and electroluminescent wire to light up, etc). In the embodiment of Figure 2A, the load may correspond to a particular device, complement, or element, such as, for example, an electroluminescent wire or an L.E.D.

According to a specific embodiment, each port of the APD device may include one or more input slots or receptacles for receiving connections to external devices, complements, and/or elements.

As shown in Figure 2A, one or more switching devices 207 (e.g. 207a, 207n) may be provided in order to individually control the flow of power and/or current two selected ports. For example, in a specific implementation, a separate switching device may be provided for each respective port of the APD device. Control of each of the switching devices may be accomplished via respective control lines 206 (e.g. control line 206a, 206n) using one or more control signals. According to a specific

embodiment, the control signals may be provided, for example, by the Active Port Detection Circuit 130 or the sequencer 110 of Figure 1.

According to a specific implementation, when a load is connected to one of the ports (e.g. port 208a), a current may flow from power source (203) through a switch (207a) to ground (209) and back through the Current Sensor (205), then back to the RETURN (204) of the power converter. When this current is flowing, the Active-Port Detect Output (220) may output a signal indicating that a device is connected to port 208a.

According to a specific embodiment, the testing of each port as either an active or inactive port may be accomplished in a serial manner, wherein power is provided to each port, one port at a time. For example, in one implementation, a "turn-on" control signal may be applied to (via control lines 206) each switch (207), one switch at a time. A circuit (e.g. the Active Port Detection Circuit 130, Figure 1) reading the Active-Port Detect Output (220) may then determine if a device is connected to the port associated with the currently selected switch. In one implementation, the circuit reading the Active-Port Detect Output (220) may correlate the "turn-on" signal with the Active-Port Detect Output (220) in order to make a map (e.g. Table 500 of FIGURE 5) of the ports to which devices are connected. Using this map, the circuit can commence to control only those ports connected to devices and ignore ports which have no device connected to them.

One advantage of detecting the presence of a device connected to a port using a current path (e.g. 204) to the power converter (202) common to all ports is that only one active-port detector circuit is needed to detect a device connected to any ports of the circuit 200.

In one embodiment (as shown, for example, in Figure 2A), the Current Sensor (205) is placed between RETURN (204) and ground (209). In another embodiment (as shown, for example, in Figure 2B), the Current Sensor (205) is placed between POWER (203) and DEVICE SUPPLY (211). The specific embodiment to be used may be determined by the devices used to perform current-detection. In the embodiments of Figures 2A and 2B, each of the APD devices has being configured to utilize a current-detection technique to detect the presence of current flowing from the Power Converter (202) to one or more of the devices connected to ports 208.

Figure 3 shows a schematic diagram illustrating a specific embodiment of the active port detection device 300 of the present invention. According to specific embodiments, the active port detection technique of the present invention may be implemented upon the occurrence of a Power ON or Reset of the APD device, or at other times desired by the user. Once the identification of active ports has been accomplished, the APD device may then commence with sequencing and/or controlling the active ports according to a predetermined sequencing pattern.

According to a specific implementation, the technique of the present invention may be used to detect the presence of electroluminescent wire connected to one or more ports 315 (e.g. 315a, 315n) of circuit illustrated in Figure 3. In the embodiment of Figure 3, the circuit 300 is supplied with an AC voltage via a DC to AC inverter (302). One output terminal of this inverter is connected to input line HVIN 304. The other output terminal of the inverter is connected to a common line HVCOM 305. The name HVCOM refers to the fact that current flowing through any wire has a common path to ground (314) via line 305, and that, according to a specific embodiment, the current flowing through any port may be detected along this path.

As shown in the embodiment of Figure 3, the APD device 300 includes a plurality of ports 315 (e.g. 315a, 315n). Each of the ports 315 is configured to include one or more receptacles or sockets. In the embodiment of FIGURE 3, each port is configured to include a receptacle having two connectors (e.g. 317a, 317b). One of the connectors (e.g. 317a) is electrically coupled to the HVIN line 304, and the other connector (e.g. 317b) is electrically coupled to a respective TRIAC 316 (e.g. 316a, 316n) which provides an electrical path for allowing current to flow from the port to ground 314. When an electrical connection is made between connectors 317a and 317b, AC current may then flow from HVIN, through the electrical connection, and back to ground (314).

According to a specific embodiment, in order to implement active port detection, an input signal may be applied to a selected control input line, such as, for example, Control Input Line 1 (318a). According to one implementation, the voltage of the input signal should preferably be sufficient to cause the TRIAC 316a to latch. In a specific implementation, the TRIAC may be configured to latch at 5mA of positive current flowing from power source 301 into the TRIAC through the resistor RW1.

According to a specific embodiment, the input signal may be applied to one TRIAC at a given instant. Each TRIAC (316) in the circuit, in turn, is given a turn-on signal in order to test whether its associated port is active or inactive. According to a specific implementation, active port detection may be implemented initially upon the occurrence of a POWER ON or RESET operation.

The sensing of the presence or absence of an external load (e.g. external element, component, circuit, etc.) connected to a particular port is commenced after the input signal is applied to its associated TRIAC. Sensing may be performed for each port (315a-n) by a sensing device, such as, for example, the Active Port Detection Circuit 130 of Figure 1. In one implementation, the sensing device may be configured to sense the current returning to ground (314) that is flowing through the load, which is connected to the port (315a) that the TRIAC (316a) controls. In this way, the sensing device is able to detect a capacitive load across the connectors (e.g. 317a, 317b) of the port. Additionally, using this technique, the sensing device is also able to detect a resistive load and/or an inductive load across the connectors (e.g. 317a, 317b) of the port.

Current flowing through HV COM (305) to and from ground (314) produces a voltage across R9, D1, and D2. Given the fact that there is a slight capacitive coupling of current between the terminals of a socket even with no wire plugged in, a false-detect can occur if this leakage current is not given a sufficient path to prevent the turning on of the detect-transistor (Q1).

For example, if R9 did not exist, then D1 and D2 would produce +/- 0.7V of potential between HVCOM (305) and Ground (314). A +0.7 V potential with regards to ground is sufficient to switch Q1 on, initiating a wire-detect, which condition is described below. By selecting R9 so that the leakage current produces much less than 0.7 V of potential via the relation ($R = I/V$), false wire-detects are thus prevented by the component R9. In a specific implementation, the value of R9 is 470 Ohms.

Diodes D1 and D2 prevent the voltage between HVCOM (305) and Ground (314) from going outside of the range +/- 0.7V. This prevents the active port detection circuit from dissipating a significant portion of the power produced by the inverter. For example, with an RMS voltage of 100V AC produced by the inverter, the 0.7V drop across D1 and D2 is $0.7V/100V * 100\text{percent} = 0.7 \text{ percent}$ of the inverter power.

Without the diodes, perhaps several volts would be present between HVCOM and Ground, leading to a several percent loss in power that is not delivered to the port being tested, and hence the load.

When an element is connected to a selected port (e.g. 315a) and the TRIAC (316a) for that port is switched on, the current flow into HVCOM (305) produces a voltage with respect to Ground (314) sufficient to switch Q1 on during the positive part of the current cycle or wave supplied by the inverter (302). This, in turn, causes C6 to be discharged to close to zero volts (0 to 0.2V). During the negative part of the current cycle of the inverter (302), C6 charges back toward 5V (180) because Q1 is now turned off and the capacitor only supplied with current from R8. However, C6 is reset to zero volts before it can rise to a logical 1 (e.g. logical 1 = 1 volt, reset occurs at about 0.5 volt) by the next positive portion of the current wave. If the capacitor C6 were not present, the wire output detect voltage at 313 would instantaneously go back to 5V, falsely indicating that no wire is present. According to a specific embodiment, the presence of a wire at the port is sensed by a logical zero (0 to 0.2V with respect to ground) at the wire detect terminal 313.

The absence of a wire is detected by waiting a sufficient amount of time (e.g. 1 ms, 2 wave cycles) for C6 to be charged up to or past a logical 1 (1.0V or greater with regards to ground 314), and hence for the wire-detect output 313 to be at a logical 1. Note that this time should preferably be greater than a half-wave cycle lest a previous wire-detect left capacitor C6 discharged and it has not charged up to a logical 1 yet. Thus, according to a specific embodiment, 2 or more wave cycles of delay occurs between the turning on of a control signal at 318 and the checking of the Wire Detect output at 313.

According to a specific implementation, the various complements of the circuit illustrated in Figure 3 may have the following corresponding values:

One other embodiment of this flow chart is to return to the wire detect procedure at periodic intervals to maintain a continuous sequence in the event of dynamic hardware failure or alteration. For example, wires could be added or removed, these changes automatically detected, and then the sequence patterns automatically adjusted. Conversely, in the first manifestation, after the table 500 has been constructed, active wires can be removed to create new patterns with blank or "dark" spaces.

Zero-Crossing Detection

The present inventive entity currently produces several produces which switch electroluminescent wire on at a speeds of 30-100Hz. Electroluminescent wire (distributed under the tradename Coolneon™ by Funhouse Productions, of Oakland, California) is generally known to one having ordinary skill in the art, and is described in greater detail in U.S. patent number 5,869,930, to Baumberg, et. al, and entitled "Electroluminescent Light Source With A Mixture Layer Filled With A Transparent Filler Substance", and U.S. patent number 5,485,355, to Voskoboinik , et al., and entitled, "Electroluminescent Light Sources", the disclosures of which are herein incorporated by reference in their entirety for all purposes.

It has been determined that when the load (e.g. electroluminescent wire) is switched sufficiently fast by an inverter (e.g. greater than 10 times per second), the inverter oscillation will periodically attenuate suddenly to 0 VRMS. The inverters recover from this situation and begin oscillating anew after at least 10-20mS, sometimes more. This time period of 10-20 mS when the inverter is at 0VRMS means that the wire being powered by the inverter perceptibly dims or flickers. This is percieved as 'wrong' or 'irritating' to a user who is expecting a regular pattern, and is especially enoticable when an inverter is being switched, for example, at 30-60Hz.

The present inventive entity has discovered that when a TRIAC turns on a wire when the inverter is not moving towards 0V, attenuation of its oscillation may occur.

It has also been discovered that when a TRIAC is turned on just before the zero-crossing of the current wave (corresponding to the AC current flowing through the wire), that an inverter will not die-down to 0VRMS, but rather will continue oscillating normally.

According to a specific embodiment, the wire-detection circuit of Figures 1 and 2 may be modified in the following way so that it not only detects a wire, but also provides zero-crossing information to the device that the wire-detect output goes to.

Figure 6 shows an example of an alternate implementation of the wire-detect circuit of Figure 2A. As shown in Figure 6, an optoisolator (609) is used to detect current flow. Additionally, there are four diodes instead of two. This is because the optoisolator's photo L.E.D. turn on voltage is around 1.4V, or 2 diode voltage drops, whereas the sequencer circuit of Figure 2A utilizes a normal transistor which turns on at approximately one diode voltage drop. The optoisolator 609 frees up the circuit to sense current off the HV Supply or HV Return, it does not matter which.

Referring to Figure 6, when no wire is plugged into any port, a slight leakage current will still flow through the diodes D1 (604), D2 (605), D3 (606) and D4 (607). R1 (608) is selected by the relation $R \ll V/I$, where V = turn on voltage of photodiode of the optoisolator (609), and I = maximum leakage current. In this way, false-detects are prevented, the same as in Fig. 2. According to a specific implementation, the value of R1 is 470 ohms.

One change to the wire-sense circuit of Figure 6 is that the charge capacitor of Figure 2A has been removed from the circuit. The circuit may be the same in all other aspects. The change is in the interpretation of the voltage levels at the Wire Detect Output (612):

When the Wire Detect Output (612) stays at 5Volts for greater than or equal to one wave-cycle after an attempt is made to turn on a wire, there is no wire plugged into the port for that wire. If, however, the Wire Detect Output is a Square Wave (of 1 wave cycle in duration) swinging, for example, from 0V to 5V, then a wire is detected. In addition, for example, the square-wave gives information about when the zero-current-crossing occurs. By timing the zero crossing of a wire, the next wire can be switched on and the current wire off just before (1-5% of phase before) the actual zero-crossing event occurs. This has been determined to remove inverter die-down (attenuation of inverter oscillation to approximately 0Vrms).

When a wire is present and under control (i.e., the TRIAC (616a) controlling it is turned on via a control signal (618a)), the photodiode of the optoisolator (609) is excited when the voltage wave of HVSUPPLY is greater than 1.5V, causing the

